What is claimed is:

1. A digital-to-analog converter comprising:

a differential transistor pair comprising a first input/output transistor and a second input/output transistor, the first input/output transistor and the second input/output transistor having an input terminal, an output terminal and a third terminal, the differential transistor pair receiving a differential logic signal at the input terminals of the first input/output transistor and the second input/output transistor;

a bistable circuit connected with the output terminal of the first input/output transistor and the output terminal of the second input/output transistor;

a clock circuit comprising a first clock transistor and a second clock transistor connected as a differential pair, the first clock transistor and the second clock transistor having a clock input terminal, a clock second terminal, and a clock third terminal, the clock second terminal of the first clock transistor being connected with the third terminal of the first and second input/output transistor, and the clock second terminal of the second clock transistor being connected with the bistable circuit; and

a current source connected with the clock third terminal of the first clock transistor and the clock third terminal of the second clock transistor, wherein:

the clock circuit acts as a switch, controlling the converter so as to provide current from the current source either to the differential transistor pair or to the bistable circuit; and

the input terminals of the first and second input/output transistor receive signals switching between a first logic value and a second logic value, switching between the first logic value and the second logic value occurring when the clock circuit controls the converter so as to provide current from the current source to the bistable circuit, said switching being asserted at the output terminal of the first and second input/output transistor when the clock circuit controls the converter so as to provide current from the current source to the differential transistor pair.

2. The converter of claim 1, wherein the first logic value and the second logic value of the signals received by the input terminals of the first and second input/output transistor are voltage values and output values of the output terminals of the first and second input/output transistor are current values.

3. The converter of claim 1, further comprising a first resistor connected with the output terminal of the first input/output transistor and a second resistor connected with the output terminal of the second input/output transistor.

4. The converter of claim 3, further comprising a cascode circuit connected with the first and second resistor.

5. The converter of claim 1, wherein the first input/output transistor, second input/output transistor, first clock transistor, and second clock transistor are selected from the group comprising npn transistors, pnp transistors, FET transistors, nMOS transistors, pMOS transistors, CMOS transistors, and MEMS switches.

6. The converter of claim 1, wherein the bistable circuit comprises a first bistable circuit transistor and a second bistable circuit transistor connected as a differential pair, the first and second bistable circuit transistor comprising a bistable circuit first terminal, a bistable circuit second terminal, and a bistable circuit third terminal.

7. The converter of claim 6, wherein the bistable circuit first terminal of the first bistable circuit transistor and the bistable circuit second terminal of the second bistable circuit transistor are connected with the output terminal of the second input/output transistor and the bistable circuit first terminal of the second bistable circuit transistor and the bistable circuit second terminal of the first bistable circuit transistor are connected with the output terminal of the first input/output transistor, and the bistable circuit third terminal of the first and second bistable circuit transistor are connected with the second clock transistor.

8. A digital-to-analog conversion method comprising:

connecting a first transistor and a second transistor as a differential pair, the first transistor and the second transistor having a switch input terminal, a switch output terminal and a switch third terminal, the first transistor and second transistor receiving a differential logic signal at the switch input terminals;

connecting a bistable circuit with the switch output terminal of the first transistor and the output terminal of the second transistor;

connecting a third transistor and a fourth transistor as a differential pair, the third transistor and the fourth transistor having a clock input terminal, a clock second terminal, and a clock third terminal;

connecting the clock second terminal of the third transistor with the switch third terminal of the first and second transistor;

connecting the clock second terminal of the fourth transistor with the bistable circuit;

connecting the clock third terminal of the third transistor and fourth transistor with a current source;

providing the switch input terminal of the first transistor with a first input signal and the switch input terminal of the second transistor with a second input signal complementary to the first input signal, the first and second input signals being switchable between a first logic input value and a second logic input value;

providing the clock input terminal of the third transistor with a first clock signal and the clock input terminal of the fourth transistor with a second clock signal complementary to the first clock signal; and

switching the first clock signal between a first clock value and a second clock value, the first clock value allowing the third transistor to conduct current from the current source to the first and second transistor and allowing the fourth transistor to block current from the current source to the bistable circuit, the second clock value allowing the third transistor to block current from the current source to the first and second transistor and allowing the fourth transistor to conduct current from the current source to the bistable circuit.

9. The method of claim 8, wherein the differential logic signal at the input terminals of the first and second transistor comprises an input signal switching between a first logic value and a second logic value.

10. The method of claim 9, wherein switching between the first logic value and the second logic value occurs during the second clock value of the first clock signal.

11. The method of claim 10, wherein said switching is asserted at the switch third terminal of the first and second transistor during the first clock value of the first clock signal.

12. A digital-to-analog converter comprising:

an input /output circuit receiving a digital input signal and outputting an analog output signal;

a bistable circuit connected with the input /output circuit;

a clock circuit connected with the input/output circuit and the bistable circuit; and

a current generator circuit connected with the clock circuit, wherein:

the clock circuit acts as a switch, providing current from the current generator either to the input/output circuit or to the bistable circuit;

the digital input signal is a switchable signal switching when the current generator provides current to the bistable circuit ; and

the analog output signal is a switchable signal associated with the digital input signal, the analog output signal switching when the current generator provides current to the input/output circuit.

13. The converter of claim 12, further comprising a cascode circuit connected with the input/output circuit.

14. A non-return-to-zero digital-to-analog converter comprising a single current source and having a first input, a second input and an output, wherein the first input determines how current is routed between the current source and the

output, and the second input determines when routing of the current between the current source and the output is allowed to change .

15. The digital-to-analog converter of claim 14, wherein the second input is a clock signal.

16. The digital-to-analog converter of claim 14, wherein the first input is a digital voltage input and the output is an analog current output.